WHAT IS CLAIMED IS:

1. A device for scrambling data by means of address lines, the processor having a CPU core to execute instructions of the processor and to access data through an address bus and a data bus, the device comprising:

a seed generator, connected to an address bus, for generating a seed in accordance with a specific address on the address bus;

a first parameter generator, connected to the seed generator, for generating a first parameter based on the seed;

a data scrambler, connected to a data bus, for scrambling data based on the first parameter when a CPU core is to write the data to the specific address; and

a de-scrambler, connected to the data bus, for de-scrambling the data based on the first parameter when the CPU core is to read the data from the specific address.

2. The device as claimed in claim 1, further comprising a selector, wherein when the CPU core is to write data, the selector selects data to be written to the data scrambler for scrambling and writes scrambled data to a memory, and when the CPU core is to read data, the selector selects data to be read to the de-scrambler for de-scrambling and sends the de-scrambled data to the CPU core.

3. The device as claimed in claim 2, further comprising a second parameter generator to generate a second parameter, wherein the data scrambler performs scrambling based on the first parameter and the second parameter, and the de-scrambler performs de-scrambling based on the first

parameter and the second parameter.

4. The device as claimed in claim 1, further comprising

a third parameter generator to generate a third parameter; and

an address scrambler, connected to the address bus, for scrambling addresses of the CPU core based on the third parameter when the CPU core is to access data on a specific address.

5. The device as claimed in claim 1, wherein the seed generator generates a seed based on entire or partial address on the address bus.

6. The device as claimed in claim 4, wherein the address scrambler performs scrambling based on entire or partial address on the address bus and thus generates a scrambled address.

7. The device as claimed in claim 6, wherein the address line number on the address bus equals to the address line number after the scrambling.

8. The device as claimed in claim 6, wherein the address line number on the address bus is not equal to the address line number after the scrambling.

9. A method for scrambling data by means of address lines, the processor having a CPU core to execute instructions of the processor and to access data through an address bus and a data bus, the method comprising steps:

a seed generation step, which generates a seed in accordance with a specific address on the address bus;

a first parameter generation step, which generates a first parameter

based on the seed;

a data scramble step, which scrambles data based on the first parameter when a CPU core is to write the data to the specific address; and

a de-scramble step, which de-scrambles the data based on the first parameter when the CPU core is to read the data from the specific address.

10. The method as claimed in claim 9, further comprising: a second parameter generation step after the first parameter generation step, which generates a second parameter such that the data scramble step performs scrambling based on the first parameter and the second parameter and the de-scramble step performs de-scrambling based on the first parameter and the second parameter.

11. The method as claimed in claim 9, further comprising:

a third parameter generation step, which generates a third parameter; and

an address scramble step, which performs scrambling address of the CPU core based on the third parameter when the CPU core is to access data on a specific address.

12. The method as claimed in claim 9, wherein the seed generation step generates a seed based on entire or partial address on the address bus.

13. The method as claimed in claim 11, wherein the address scramble step performs scrambling based on entire or partial address on the address bus and thus generates a scrambled address.

14. The method as claimed in claim 13, wherein the address line number on the address bus equals to the address line number after the

scrambling.

15. The method as claimed in claim 13, wherein the address line number on the address bus is not equal to the address line number after the scrambling.